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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,160	11/19/1999	DAVID L. ISAMAN	130.1012.02	6854

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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/443,160	ISAMAN, DAVID L.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,12-17,20-21* is/are rejected.

7)☒ Claim(s) *8-11,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2-21 remain for examination. Claim1 has been canceled.

2. Claims 2, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett (5,854,921) in view of Amerson (5,475,823) .

3. Claims 2-7, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson et al. (5,475,823) in view Srinivasan et al. (5,706,224) .

4. Claims 2-7, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson et al. (5,475,823) in view Pickett (5,854,921) .

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2-7, 12-17 are rejected under 35 U.S.C. 102 (b) as being anticipated by Amerson et al. (5,475,823) .

6. Claims 20,21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Engebretsen et al. (5,860, 138) in view of Ball (5,615,357).

7. The rejections are maintained and incorporated by reference the last Office action on 08/08/05.

8. The response filed on 11/14/05 has been fully considered but is not persuasive.

9. In the remarks, applicant argued that :

a) Amerson compared the actual addresses by the load and store instruction, these actual addresses must have been computed by some component in Amerson; it is impossible for Armeson to compare the actual addresses without first computing the actual addresses;

b) actual memory address in Armeson requires that the actual memory addresses be computed first . As result , the detection in Armeson does not occur without requiring computation " for the load and store;

c) Pickett did not recite address calculation was not required for operands stored in the registers;

d) no detection of instruction wherein the instruction was detected without requiring computation of an external memory address of the first memory location for the instruction;

e) nothing in Srinivasan teach the detection of instruction. Armeson did not show the use of content addressable memory;

f) the only issue is whether Ball operate without requiring computation of effective addresses for memory location

10. As to a) above, applicant is kindly reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). For example, nowhere does applicant claim recite that the memory address must not be computed first , or must be without computed first, must not require to have been computed, or the like. Applicant only claims "detecting instruction ...without requiring computation of ... memory address of said first memory location for the instruction...". The detection of Armeson involved the comparison of the load and store addresses (see col.1, lines 30-41, col.4, lines 30-37, col.5, ines 16-19, see also the instruciton detector in fig.5). Whether the address had been computed or not is irrelevant to the claimed invention (applicant did not claim that the address must not have been computed, the computation must not have been required, or the like). Armeson's detection was a logic operation (compare), not arithmetic operation. The logic operation requires no computation. For example, a logic AND is comparing whether the asserted value is the same as a predetermined value. It does not involve computation. The value might have been computed before, but at the comparison step (the detection) , no calculation was required. The fact the addresses have been calculated before is irrelevant to the claimed invention. As long as Armerson's comparison step was a logical operation, it read on the claimed "without calculating". It is also evident that when applicant emphasized the feature of "detecting" (see

applicant argument page 12, lines 16-17) , the focus is on weather to calculate the address during the comparison step(detection), not whether or not the calculation has been done before the detection, which is not even recited into the claim. The point is that even if Armeson had computed the addresses, a computation was not required at the detection stage (the comparison).

11. As to b) above, applicant is reminded that Armeson never taught that his memory address were actual address, nor must be calculated before comparison (the detection). Nevertheless, let's assume that applicant's characterization of Armeson were correct. Applicant taught a computation stage 130 to compute the effective address of the instruction (see page 13, lines 8-10). Therefore, based applicant's teaching, the actual address must be calculated.

12. As to c), Pickett did disclose no address calculation was needed to locate the operands (see col.2, lines 25-30, see also citation already included in the last Office action).

13. As to d), see reasons for obviousness in pages 2, 3 , Paragraph # 3, of the last Office action on 08/08/05.

14. As to e) , Srinivasan was used to supplement the teaching of the "without requiring calculation". The reasons of obviousness were already given in paragraph 8 of the last Office action, therefore, it will not be repeated herein. As to whether Amerson showed the use of content addressable memory, Srinivasan already taught content addressable memory had been known and used in the prior art (see col.1, lines 14-32), therefore, one of ordinary skill in the art should be able to recognize the use content addressable memory in Armeson .

15. As to f), examiner would like to rephrase applicant's argument more accurately with modification as : "the only issue is whether Ball ***determined*** (operate) without requiring computation of effective addresses for memory location" (see determination in claim 20, line 11). The claim never recites not have been required to be computed, no requirement of computation beyond or before the determination, never requiring computation, or the like. Therefore, as long as no computation occurs during the determination, it will read on the claim. Nevertheless, Ball disclosed a system including a determination of syntax relationship (see the model of CPU) without itself calculating effective addresses of the first a and second instructions (see the trace file containing the load and store instruction effective addresses in col.2, lines 39-45, lines 64-67, col.3, lines 1-6, col.4, lines 1-1 1 , col.11 , lines 59-67, see col.10, lines 10-52 for the trace driven mode, see col.12, lines 1-7 for load and store). Therefore, Ball did not

require to calculate the address. The primary reference, Engebretsen, also taught that if an instruction references a memory location , a data cache can be checked if the referenced memory location is mapped into the data cache, and if it is, there is no need to go to the memory to obtain the data (see col.2, lines 17-25), which was , therefore, a suggestion of the need for not having to calculate the memory address (for example, no need to go to the memory , therefore, no address calculation was needed) in order to increase the processing efficiency, and in doing so, provided a motivation. Moreover, a referenced address by an instruction does not necessarily mean that the address requires calculation. For example, it might be an address specified by the instruction in the instruction format. Engebretsen taught that his instruction referenced a memory location, therefore, it might be an address specified by the instruction in the instruction format, and therefore, no caluculation.

16. Claims 8,9, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitatigns of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the identical offset address value from identical base address in a register within the pipeline microprocessor.

17. Claims 10, 11 , 18,19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of instruction decoder stage for detecting load/store data from identical memory location by identifying the offset address from identical base address in a register, and the bypass signal to instruction execution stage that reference to an identical memory location.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or

the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP